

# Dissolution of Printed Circuit Board Copper Barrel Plating Found with Multiple/Extended Exposure Thermal Stress Testing

Renee J. Michalkiewicz and Scott S. Opperhauser, Trace Laboratories – East  
Hunt Valley, Maryland

Zequn Mei and Mason Hu, Cisco Systems, Inc.  
San Jose, California

## **Abstract:**

Up to a 0.0008” reduction in copper (Cu) barrel plating was found with multiple exposure thermal stress testing in accordance with IPC-TM-650, Method 2.6.8, *modified*. A typical original equipment manufacturer (OEM) specification for printed circuit board specimens specifies 3 or 6 thermal stress cycles. For boards with an initial Cu plating thickness of 0.0010” to 0.0015”, this reduction of 0.0008” is significant and may contribute to cracking in Cu plating, especially at the through-hole and pad intersection.

This report is the first in a series required to determine if copper dissolution does indeed occur in thermal stress testing and furthermore, to determine if this dissolution has any direct relevance to printed circuit board performance and reliability. The ramifications of this research may ultimately require specification changes.

## **Introduction:**

The Viking probe missions were an exciting time in America’s early quest in the race for space. The rigorous space environment demanded NASA, the government and its contractors and suppliers reinvent technologies capable of withstanding long-term exposures to the thermomechanical extremes of space travel.

The requirements imposed at materials level became what can still be considered as the leading edge for high reliability applications. Printed circuit board (PCB) material suppliers were forced to produce products with increased thermal capacity, while PC board fabricators were tasked with providing circuit boards capable of multiple thermal excursions, well beyond the thermal stresses incurred at wave soldering and subsequent assembly.

It was at this time in the early 1980’s that the National Security Agency (NSA) in Fort Meade, Maryland, initiated a program for multiple thermal stress testing at printed circuit board level. Basically, the intent was to reproduce a worst-case scenario whereby multiple repairs (in the field) would be necessary for ongoing equipment reliability. This scenario would be accomplished by utilizing five (5) sequential solder stresses at 550°F, followed by analytical surface and subsurface inspection and analysis of the cross-sectioned area. Subsequent analysis would determine the integrity of the substrate and the surrounding metals and their interconnections. Virtually all analysis was centered on the thermal attributes of the dielectrics and metal interconnections.

Some of the adverse findings of these analyses were plating separations, plating cracks and laminate defects. A dissolution of the copper plating within the plated through hole with multiple thermal stress cycles was not obvious nor within the original expected defect scope. Within the past five years, however, several original equipment manufacturers (OEM’s) have been, again, concerned with printed circuit board reliability as it relates the multiple thermal excursions. During the assembly process, it is not unusual for a board to see between three and six thermal excursions during reflow, rework and repair. It is during these subsequent studies that dissolution of copper during multiple thermal stress cycles was evidenced.

## **Background Information:**

The thermal stress test is an IPC standard test for PCB thermal reliability (IPC-TM-650, Method 2.6.8.). In a thermal stress test, a PCB sample is fluxed then floated on the top a molten solder pot at 288°C for 10 seconds. A typical OEM modification follows with a short break and floating of the PCB sample again on the solder pot. A typical product specification calls for 3 or 6 times of floating over the solder pot without any breakage or delamination in vias or the multilayer PCB structure. During this solder exposure, the copper plating on PCB samples dissolves into molten solder.

This investigation was initiated because the lab and OEM noted a possible trend in reporting of thin (less than 1.0 mil) copper plating following 6X thermal stress testing. During a three-month span ten out of the twenty-one submissions reviewed failed for isolated thin plating measuring less than 0.8 mil.

Vendor	Lots Exhibiting Thin Plating	Lots Meeting Plating Thickness Requirement
A	1	0
B	1	0
C	0	1
D	2	2
E	4	1
F	1	1
G	1	0
H	0	1
I	0	1
J	0	1
K	0	1
L	0	1
M	0	1
<b>TOTAL</b>	<b>10</b>	<b>11</b>

**Table 1 – Summary of Pass/Fail Plating Thickness Results for Thirteen Suppliers**

The investigation began with a thorough evaluation of thermal stress procedures being used within the laboratory. The following were eliminated as contributing factors relating the copper thinning:

- It was confirmed that an ROL1 flux was being used as specified in the IPC 2.6.8 test method.
- It was confirmed that the flux in-use was not beyond its shelf life.
- The temperature of the solder bath being used was confirmed using two different NIST-traceable calibrated pyrometers.
- It was confirmed that four different engineers had performed thermal stress testing on various suppliers' boards. All engineers had reported thin copper plating. Thin plating was not observed on all suppliers' product nor was it found with every part number from a specific supplier. This ruled out engineer and supplier contribution.
- There was no consistency found relating to the type of surface finish used. Finishes included Tin/Lead, Silver, Tin, and OSP.
- It was confirmed that pressure was not being placed to the top of the sample which was thought to be a possible cause.
- This particular OEM specification does not call for fluxing in between solder floats, so this was eliminated as a possible cause.
- Contamination limits of the solder bath in-use were found to be acceptable (see Table 2). Results are a combination of internal evaluations and outsourced evaluations. This negates the possibility of erroneous atomic absorption / inductively coupled plasma (AA/ICP) results. Because copper is the metal being dissolved during testing, the levels are highlighted in the tables below.

Element	Requirement <sup>1</sup> (Max wt%)	12/03	1/04*	2/04	3/04
Silver (Ag)	0.100	0.006	0.005	< 0.005	< 0.005
Aluminum (Al)	0.006	< 0.005	< 0.005	< 0.005	< 0.005
Arsenic (As)	0.030	< 0.005	< 0.005	< 0.005	< 0.005
Gold (Au)	0.200	< 0.005	< 0.005	< 0.005	< 0.005
Bismuth (Bi)	0.250	0.028	0.046	0.048	0.054
Cadmium (Cd)	0.005	< 0.005	< 0.005	< 0.005	< 0.005
<b>Copper (Cu)</b>	<b>0.300</b>	<b>0.272</b>	<b>0.005*</b>	<b>0.008</b>	<b>0.012</b>
Iron (Fe)	0.020	< 0.005	< 0.005	< 0.005	< 0.005
Nickel (Ni)	0.010	< 0.005	< 0.005	< 0.005	< 0.005
Zinc (Zn)	0.005	< 0.005	< 0.005	< 0.005	< 0.005
Antimony (Sb)	0.500	< 0.005	< 0.005	< 0.005	< 0.005
Tin (Sn)	63.0 ± 1.5	63.87%	63.49%	62.86%	63.79%

Element	Requirement <sup>1</sup> (Max wt%)	4/04**	7/04	8/04	9/04
Silver (Ag)	0.100	< 0.005	< 0.005	< 0.005	< 0.005
Aluminum (Al)	0.006	< 0.005	< 0.005	< 0.005	< 0.005
Arsenic (As)	0.030	< 0.005	< 0.01	< 0.005	< 0.01
Gold (Au)	0.200	< 0.005	< 0.005	< 0.005	< 0.005
Bismuth (Bi)	0.250	0.057	< 0.005	< 0.005	< 0.005
Cadmium (Cd)	0.005	< 0.005	< 0.005	< 0.005	< 0.005
<b>Copper (Cu)</b>	<b>0.300</b>	<b>0.012</b>	<b>0.030</b>	<b>0.030</b>	<b>0.030</b>
Iron (Fe)	0.020	< 0.005	< 0.005	< 0.005	< 0.005
Nickel (Ni)	0.010	0.008	< 0.005	< 0.005	< 0.005
Zinc (Zn)	0.005	< 0.005	< 0.005	< 0.005	< 0.005
Antimony (Sb)	0.500	< 0.005	< 0.005	0.006	< 0.005
Tin (Sn)	63.0 ± 1.5	63.81%	62.46%	62.82%	62.38%

**Table 2- Solder Bath Element Concentration (wt%)**

\*Changed solder in solder bath.

\*\* Switched to quarterly measurements because values well below upper limit. QM to monitor and change to monthly when value exceeds 0.20 wt%.

Polls internally and of other industry experts lead to the following hypotheses regarding copper dissolution during multiple thermal stresses:

1. Due to the fact that you can never truly microsection the same exact holes in the as-received and thermal stress conditions, it is coincidence that thin plating is only being observed in the thermal stress condition.
  - a. Often, underlying causes for the thin plating (foil, subsurface strike, dielectric and/or barrel issues) were observed.
  - b. Copper plating thicknesses in through-holes across the board vary due to the presence of high and low current density areas.<sup>1</sup>
2. An increase in organic material in the solder bath can lead to dissolution of copper into solution.
3. The solubility of the copper is most vulnerable to dissolution when the bath is new. This hypothesis is loosely based on the knowledge that drinking water tends to leach copper ions from copper piping.<sup>2</sup>
4. The copper plating chemistry used in the board manufacturing process is causing the dissolution of copper observed on particular lots.
5. A combination of hypotheses three and four are the cause.

Additionally, a literature search was performed and little information was found relating to this topic specifically. Work initially reported in the 1960's by Bader and since referenced often provided an empirical formula where the dissolving rate of a copper wire in a tin-lead solder bath is constant at a given temperature, and the temperature dependent dissolving rate is an Arrhenius type.<sup>3</sup> A more recent *Circuits Assembly* article authored by Willis discusses the issue of copper erosion due to new lead-free initiatives.<sup>4</sup> Again, in a study performed by Faizan, Lin, Srivatsan and Wang the focus is solely on the dissolution of copper in lead-free solder alloys, Tin and Tin-Silver.<sup>5</sup>

**Study Outline:**

The purpose of this paper is to test the validity of hypothesis number one and show whether or not there is indeed dissolution of copper occurring with multiple thermal stress cycles. One word of caution regarding the interpretation of the findings – It is not possible to prepare a microsection of the same exact hole in the as-received condition as well as the thermally stressed condition. The holes that were selected were adjacent to each other and were of the same diameter but were not the same exact hole.

Three bare boards were chosen from three separate suppliers. Two of the boards were the same part number (i.e. same design). The suppliers will be referenced as Vendor A, Vendor B and Vendor C. Vendor B and C data is from the same part number.

Similar locations were chosen from each board. Thirteen specimens were taken from each board. Specimens were labeled as 0X, 1X, 2X, 3X, 4X, 5X, and 6X. Half of each specimen was covered with plater’s tape to protect the holes from the solder exposure. The specimens were baked and tested in accordance with IPC-TM-650, Method 2.6.8 which was modified for multiple exposures. After the initial solder float, the specimen was cooled for 120 seconds and again floated on the solder pot with no additional fluxing between floats. Following stressing, the pieces were microsectioned in accordance with IPC-TM-650, Method 2.1.1. This testing was completed in August 04. Refer to Table 1 for solder bath contaminant levels at the time of testing.

Each evaluation (1X – covered, 1X – uncovered, 2X – covered, etc.) included measurements of six plated through holes. The average copper plating reported below is the average value of these six holes. The average for each hole is determined by measuring the plating thickness at the top, middle, and bottom of the hole on each side of the barrel. The Isolated Thinning, reported below, is the thinnest measurement observed for each set of holes. This thinning was most often observed at the pad – through-hole intersect (I.e. Knee area).

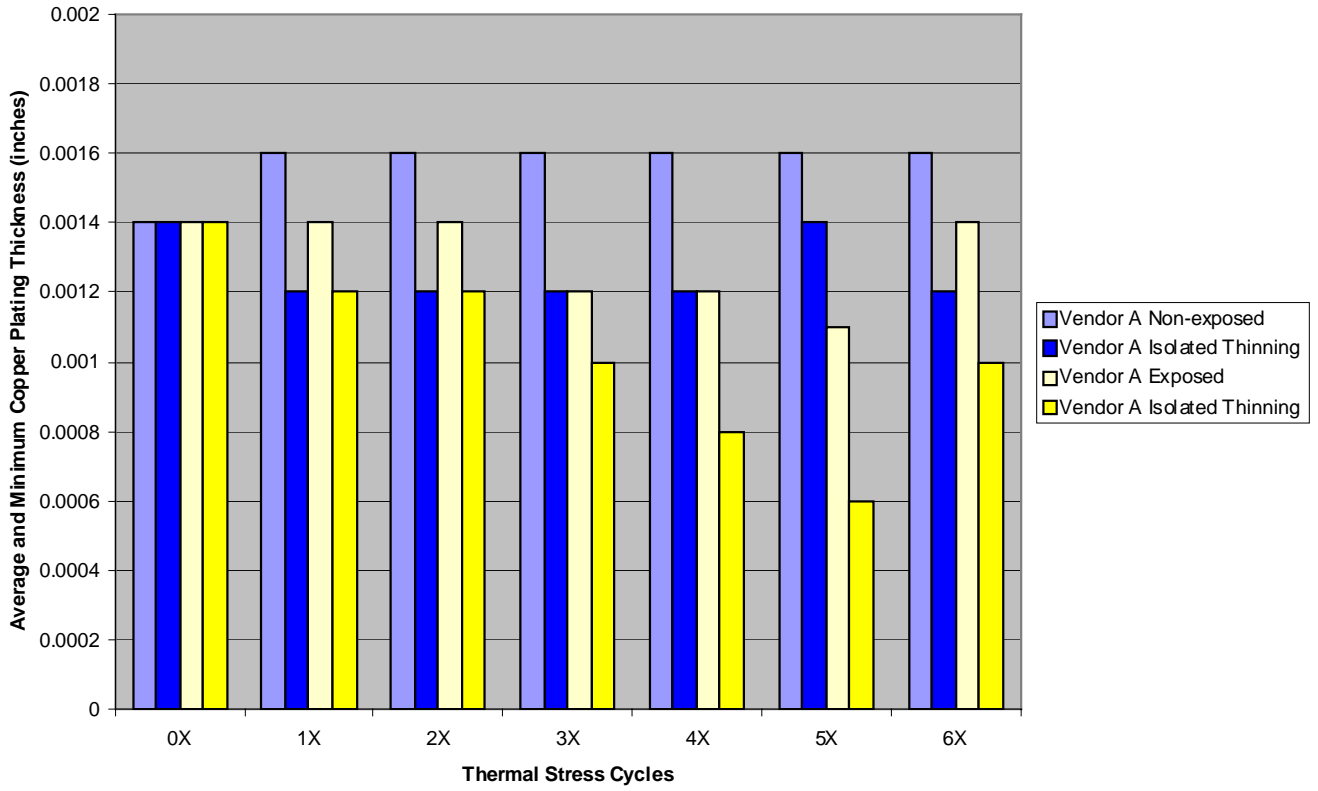
**Discussion of Vendor A Results:**

A reduction in average copper plating thickness of 0.2mil was found at 1X thermal stress. The maximum reduction in the average was observed at 5X and measured 0.5mil. A reduction at the knee (Isolated thinning) of 0.8mil was found at 5X thermal stress cycles. This value of 0.6mil failed to meet the OEM specification and was cause for rejection. See Table 3, Figure 1 and photos 1-13, below. Figure 1 at 2X through 5X shows the only real linear trend observed in plating reduction although the 6X value does not fall in line with the curve.

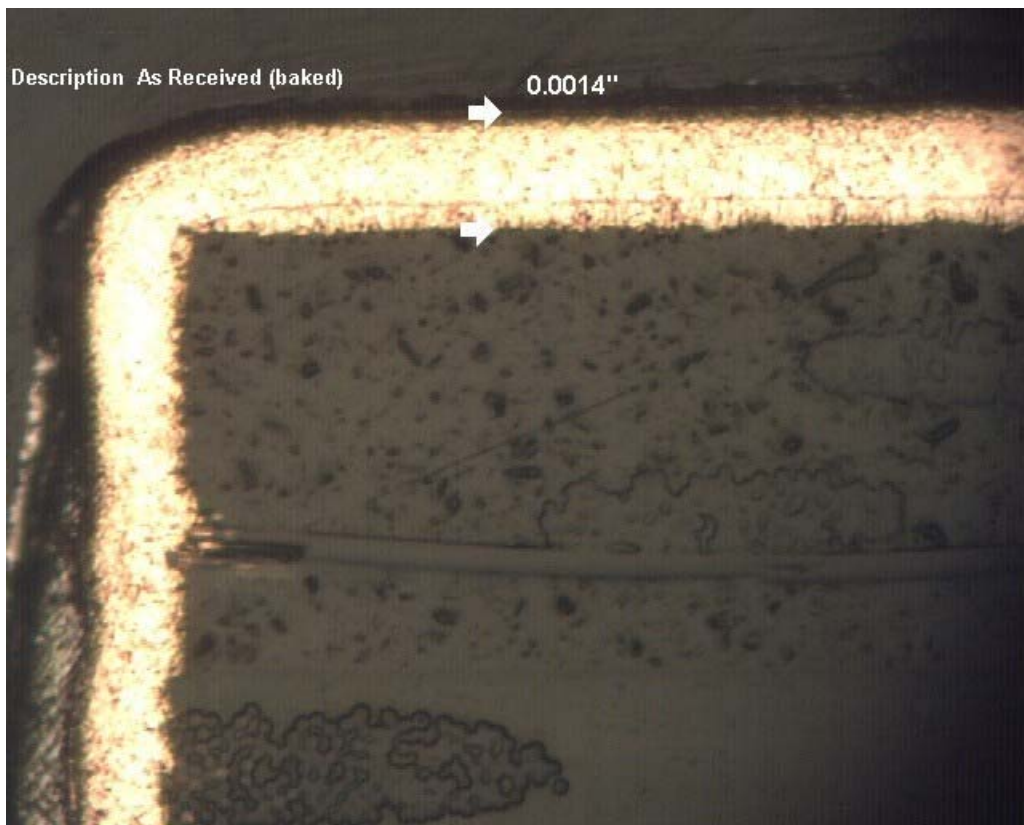
	Vendor A					
	Non-exposed Average Copper Plating	Exposed Average Copper Plating	Reduction in Average Copper Plating	Isolated Thinning (Non-Exposed)	Isolated Thinning (Exposed)	Reduction
0X	0.0014	0.0014	0.0000	0.0014	0.0014	0.0000
1X	0.0016	0.0014	0.0002	0.0012	0.0012	0.0000
2X	0.0016	0.0014	0.0002	0.0012	0.0012	0.0000
3X	0.0016	0.0012	0.0004	0.0012	0.0010	0.0002
4X	0.0016	0.0012	0.0004	0.0012	0.0008	0.0004
5X	0.0016	0.0011	0.0005	0.0014	0.0006	0.0008
6X	0.0016	0.0014	0.0002	0.0012	0.0010	0.0002

**Table 3: Vendor A Through hole plating measurements in inches.**

**Vendor A - 0X to 6X Thermal Stress**



**Figure 1: Graph of Table 3 Data**



**Photo 1: Vendor A, 0X Thermal Stress**

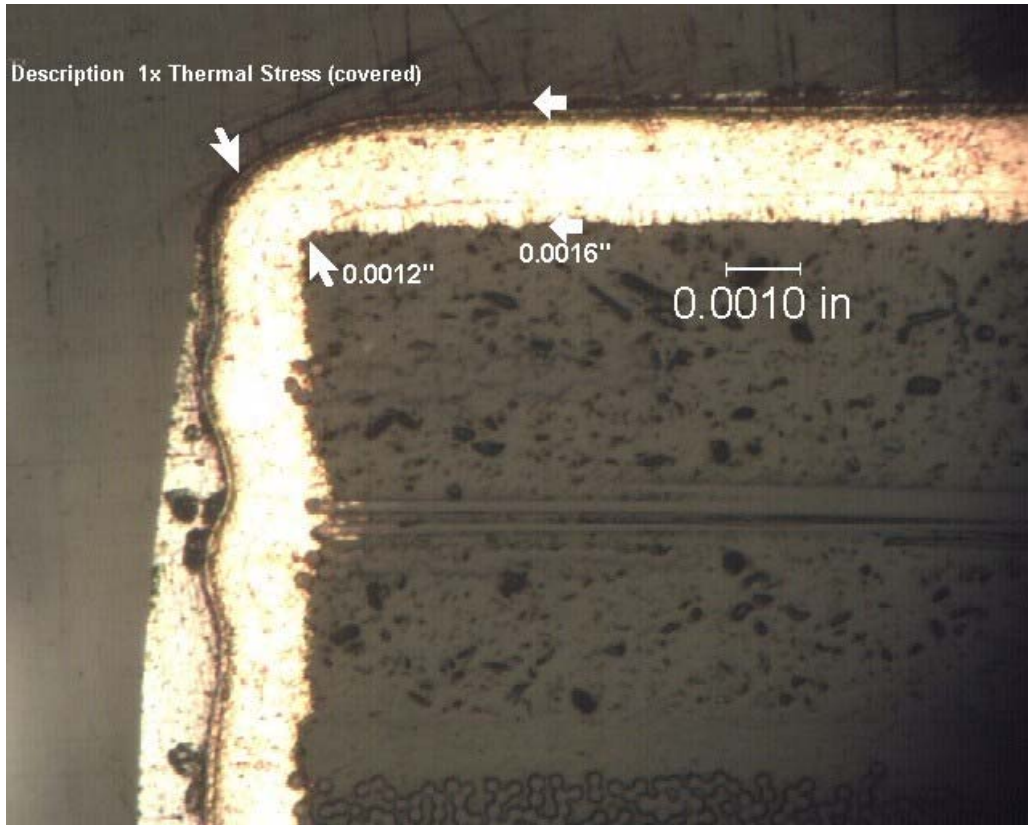


Photo 2: Vendor A, 1X Thermal Stress Covered

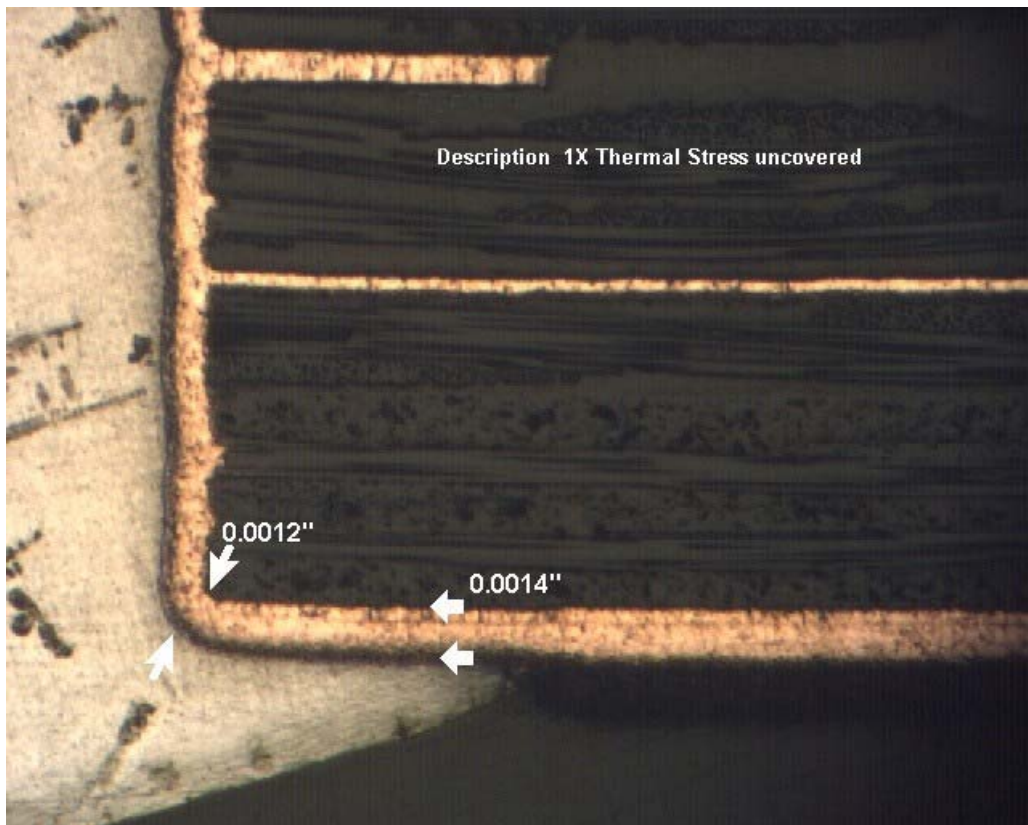
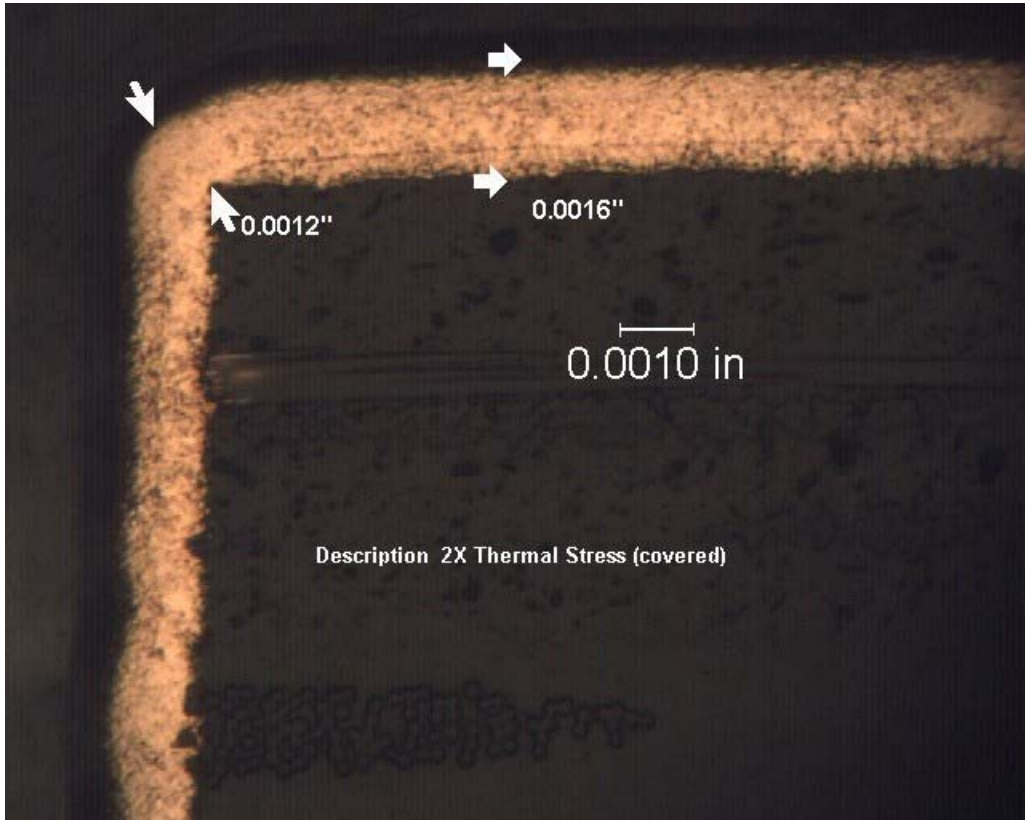


Photo 3: Vendor A, 1X Thermal Stress, Uncovered



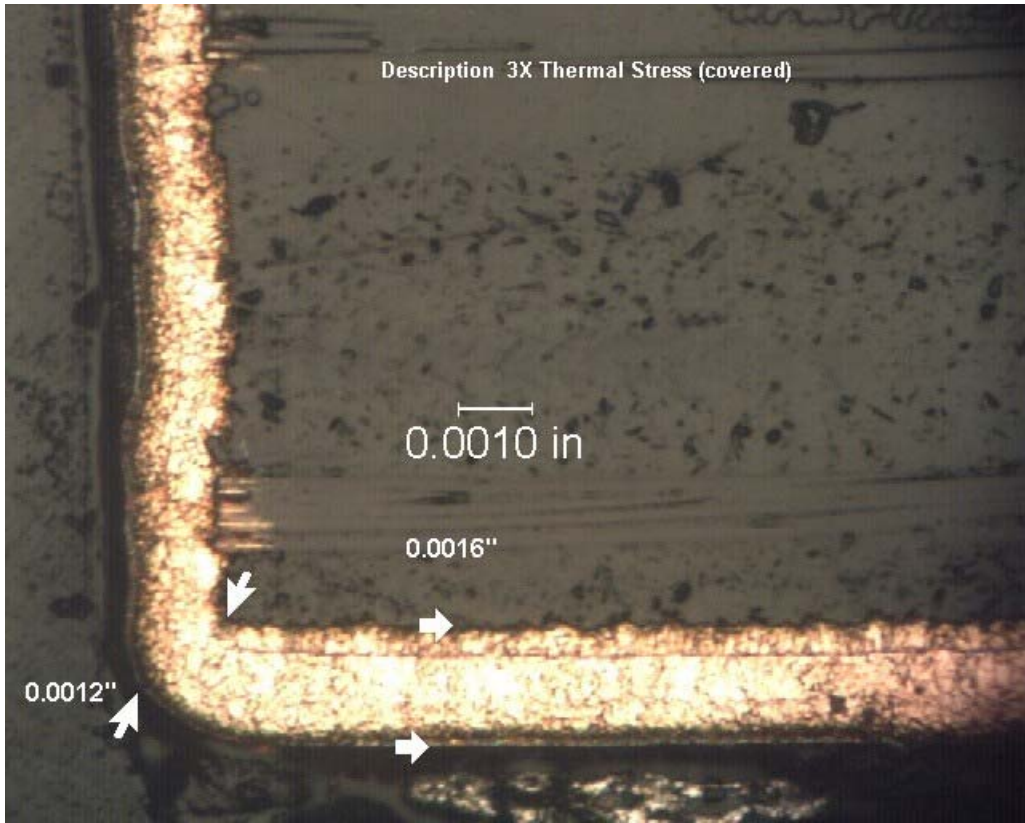


**Photo 4: Vendor A, 2X Thermal Stress, Covered**

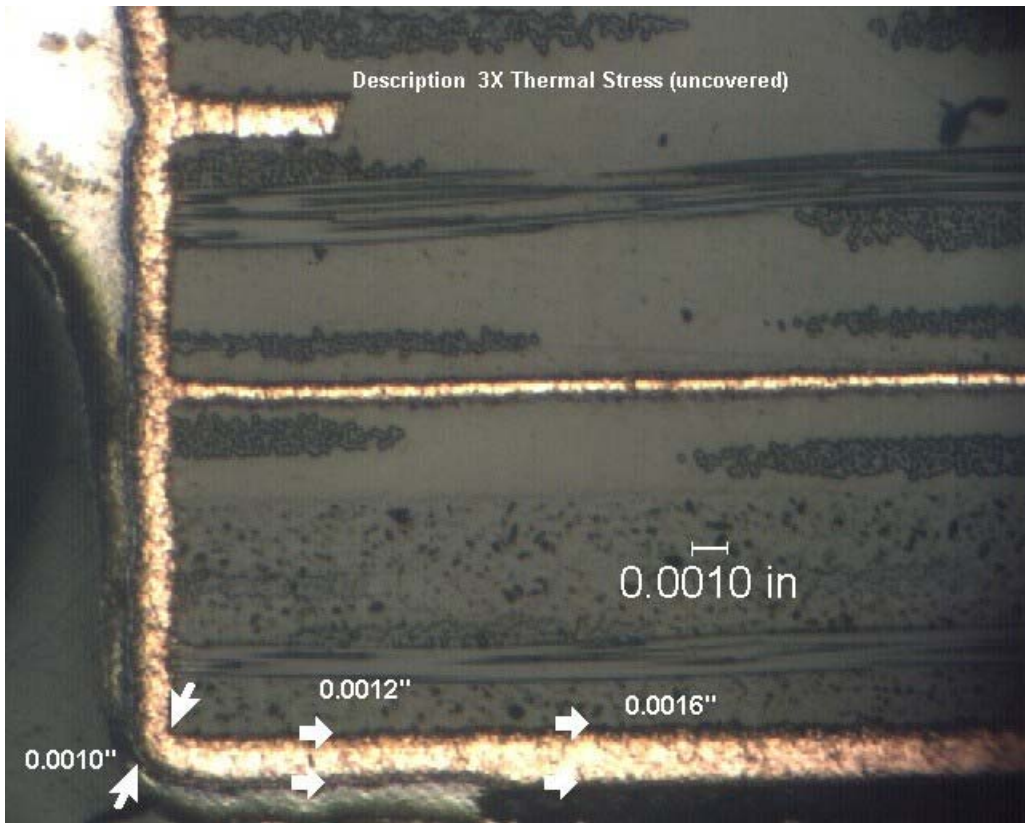


**Photo 5: Vendor A, 2X Thermal Stress, Uncovered**

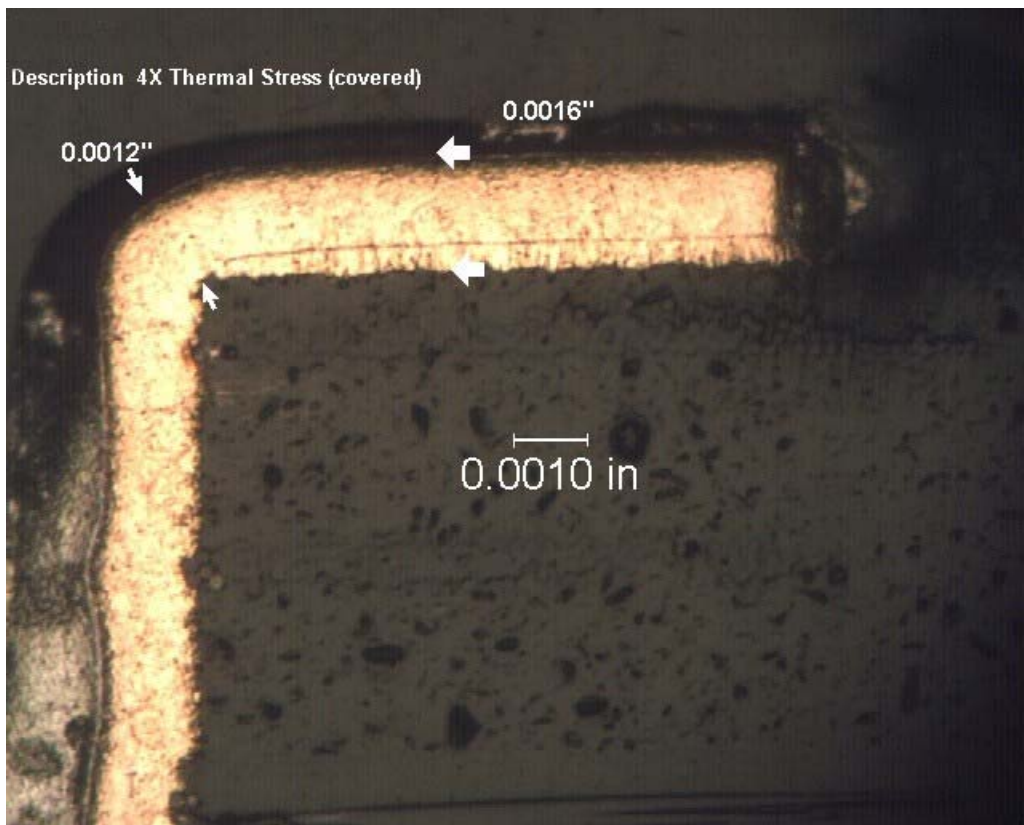




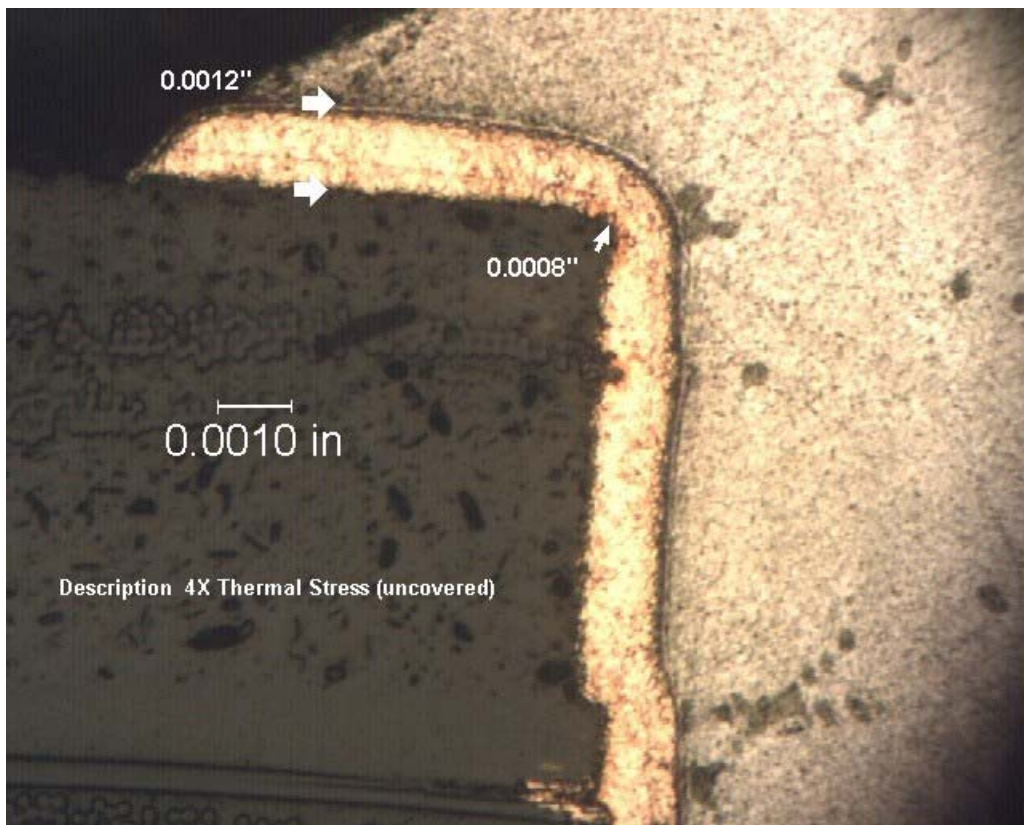
**Photo 6: Vendor A, 3X Thermal Stress, Covered**



**Photo 7: Vendor A, 3X Thermal Stress, Uncovered**

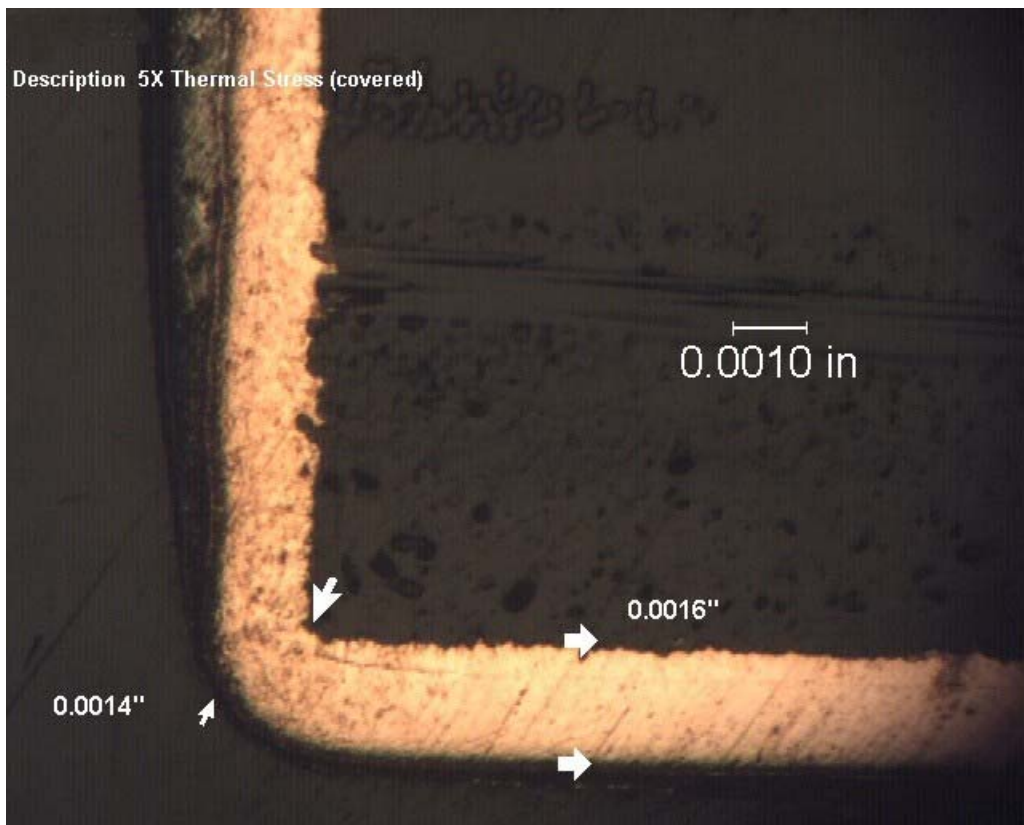


**Photo 8: Vendor A, 4X Thermal Stress, Covered**

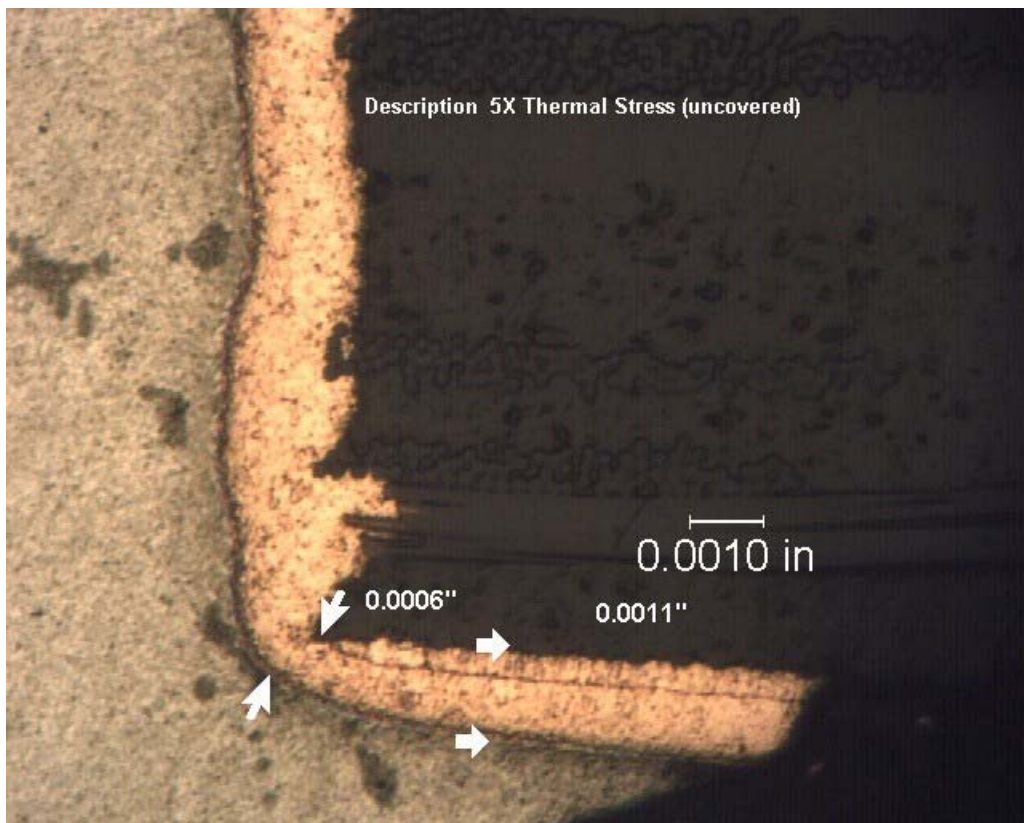


**Photo 9: Vendor A, 4X Thermal Stress, Uncovered**

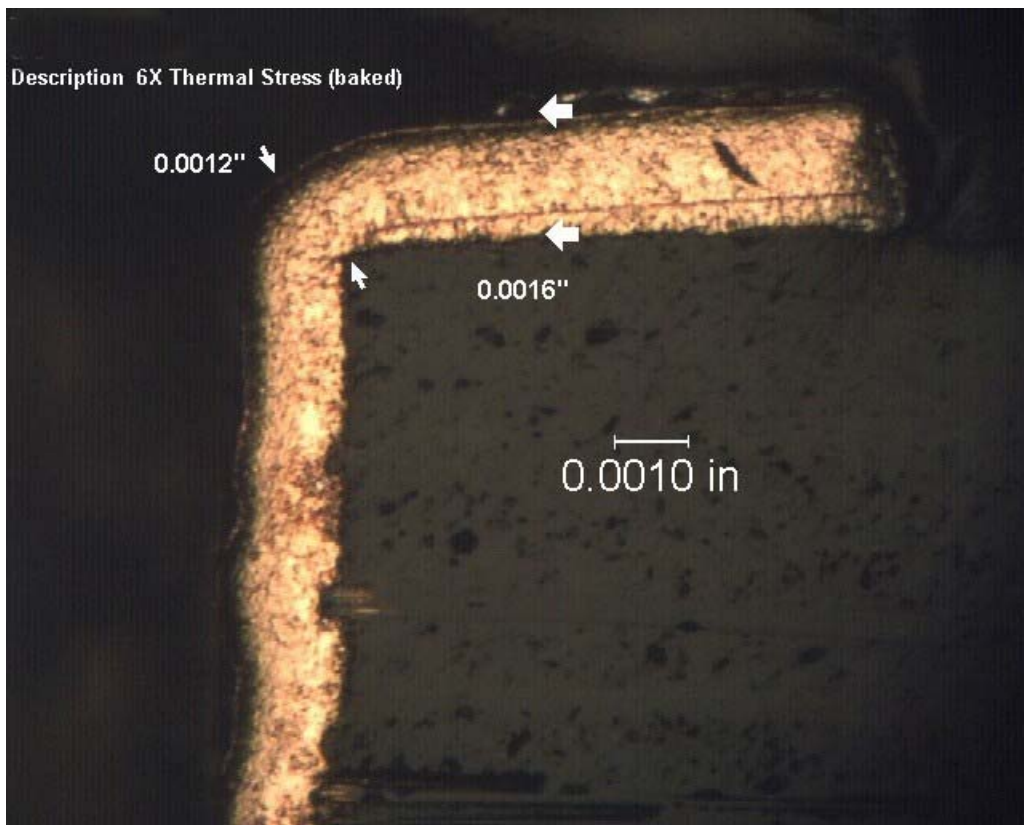




**Photo 10: Vendor A, 5X Thermal Stress, Covered**



**Photo 11: Vendor A, 5X Thermal Stress, Uncovered, Showing Thinning at the Knee Below Minimum Requirements**



**Photo 12: Vendor A, 6X Thermal Stress, Covered**



**Photo 13: Vendor A, 6X Thermal Stress, Uncovered**

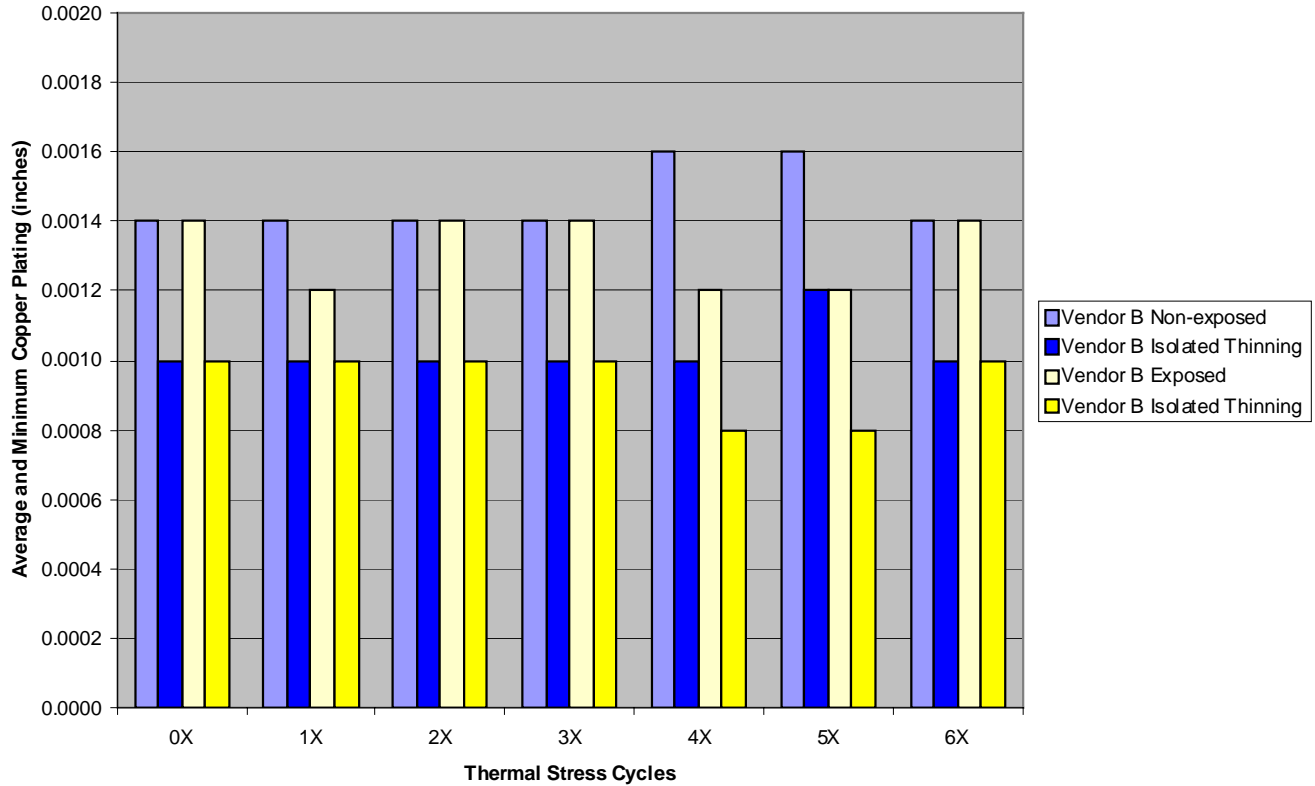
**Discussion of Vendor B Results:**

A reduction in average copper plating thickness of 0.2mil was found at 1X thermal stress. The maximum reduction in the average was observed at 4 and 5X and measured 0.4mil. Results from this study did not lead to rejection of the product, although when initially tested this product was rejected due to isolated thinning at the knee measuring less than 0.8mil. See Table 4 and Figure 2.

	Vendor B					
	Non-exposed Average Copper Plating	Exposed Average Copper Plating	Reduction in Average Copper Plating	Isolated Thinning (Non-Exposed)	Isolated Thinning (Exposed)	Reduction
0X	0.0014	0.0014	0.0000	0.0010	0.0010	0.0000
1X	0.0014	0.0012	0.0002	0.0010	0.0010	0.0000
2X	0.0014	0.0014	0.0000	0.0010	0.0010	0.0000
3X	0.0014	0.0014	0.0000	0.0010	0.0010	0.0000
4X	0.0016	0.0012	0.0004	0.0010	0.0008	0.0002
5X	0.0016	0.0012	0.0004	0.0012	0.0008	0.0004
6X	0.0014	0.0014	0.0000	0.0010	0.0010	0.0000

**Table 4: Vendor B Through hole plating measurements in inches.**

**Vendor B - 0x to 6X Thermal Stress**



**Figure 2: Graph of Table 4 Data**

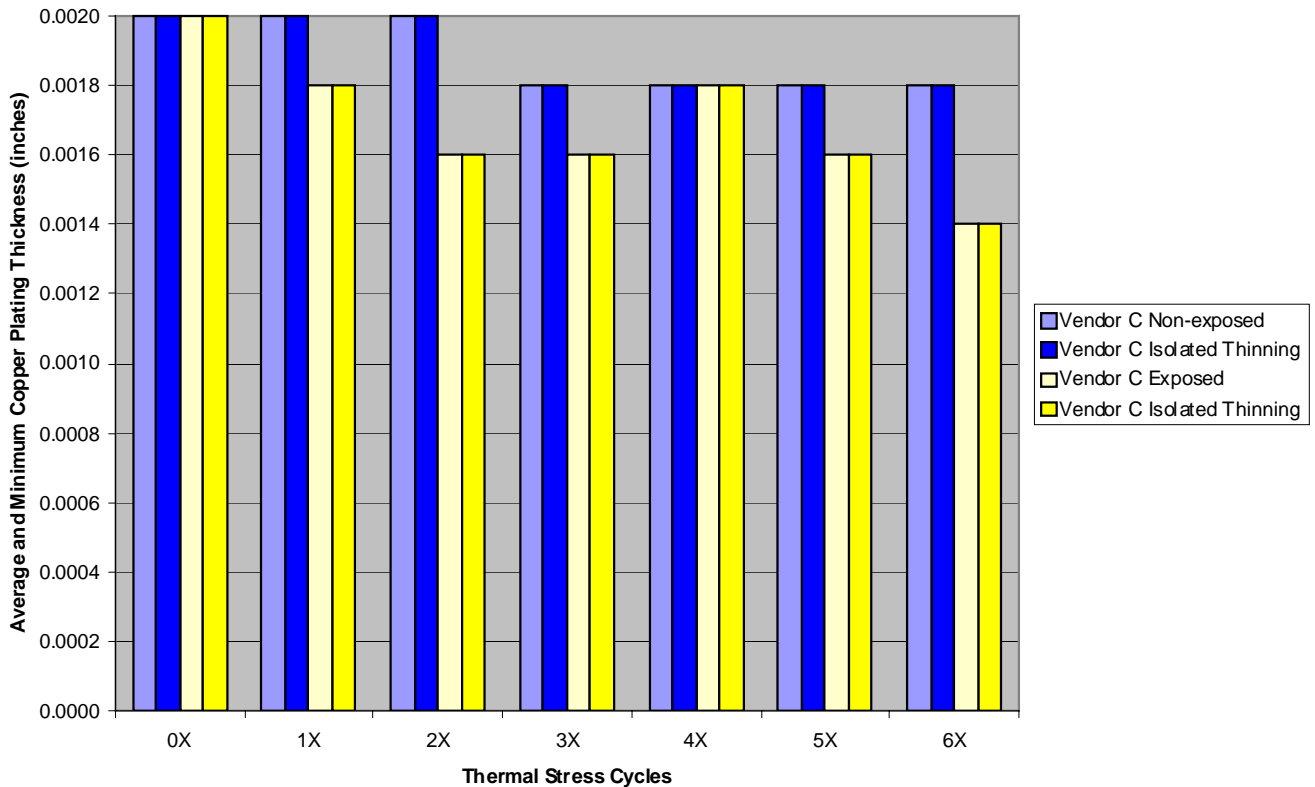
**Discussion of Vendor C Results:**

A reduction in average copper plating thickness of 0.2mil was found at 1X thermal stress. The maximum reduction in the average was observed at 2 and 6X and measured 0.4mil. The initial plating thickness of 1.8 to 2.0mils was well above the minimum requirement; therefore, the loss of copper thickness did not lead to rejection of the product. . See Table 5 and Figure 3.

	Vendor C					
	Non-exposed Average Copper Plating	Exposed Average Copper Plating	Reduction in Average Copper Plating	Isolated Thinning	Isolated Thinning	Reduction
0X	0.0020	0.0020	0.0000	0.0020	0.0020	0.0000
1X	0.0020	0.0018	0.0002	0.0020	0.0018	0.0002
2X	0.0020	0.0016	0.0004	0.0020	0.0016	0.0004
3X	0.0018	0.0016	0.0002	0.0018	0.0016	0.0002
4X	0.0018	0.0018	0.0000	0.0018	0.0018	0.0000
5X	0.0018	0.0016	0.0002	0.0018	0.0016	0.0002
6X	0.0018	0.0014	0.0004	0.0018	0.0014	0.0004

**Table 5: Vendor C Through hole plating measurements in inches.**

**Vendor C - 0X to 6X Thermal Stress**



**Figure 3: Graph of Table 5 Data**



***Conclusions:***

It was found in this study that through-hole copper plating thickness may be reduced by as much as 0.8 mil when a PCB is floated over a solder pot at 288°C for 6 thermal cycles. For an initial copper plating thickness of 1 to 2 mils, this reduction of 0.8mil is significant and may contribute to cracking in the copper barrel plating, especially at the location where through-hole and pad intersect (i.e. the knee area). It may be argued that PCB's will never see six solder exposures, hence negating the relevance of these results. But one needs to consider boards where the initial plating thickness is at the minimum requirements (1.0mil average with 0.8mil isolated thinning) where as little as a 1X thermal stress cycle can lead to thin plating and contribute to cracking, yet as-received plating measurements are within specification requirements.

Questions that will be considered for future papers include the following:

- Does an increase in organic material in the solder bath lead to dissolution of copper into solution?
- Is the solubility of the copper most vulnerable to dissolution when the solder bath is new?
- Does the copper plating chemistry used in the board manufacturing process have any effect on the rate of copper dissolution?
- Do adverse results of the multiple thermal stress test correlate with short or long term product reliability issues?

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## End Notes

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5. Faizan, M., Lin, D., Srivatsan, T.S., and Wang, G.X. (2003) Study of Copper Dissolution and Formation of Intermetallic Compound in Molten Sn and Sn-Ag Solder. Proceedings of 2003 ASME Summer Heat Transfer Conference.